VLN3M Series

32-bit Voice IC in SOP-16

Version 1.9

May. 17, 2019

1. GENERAL DESCRIPTION

The VLN3M series is a 32-bit MCU based high-quality speech/MIDI processor, which is specially designed for customers to innovate with advanced DSP power. It is embedded with OTP (One Time PROM) for mass production, such that no mask is required while MOQ / Lead Time are kept minimized.

With Instruction / Data Local Memory bus (ILM/DLM) built in CPU, the VLN3M can run 1.57 DMIPS per MHz and up to 50+ DMIPS @ 32MHz. In addition, the dual clock design let customers switch between fast / slow clocks for achieving the best power consumption and performance ratio, or may employ 32.768KHz X'tal oscillator for time-keeping applications.

The VLN3M series consists of several derivatives with respect to ROM (OTP), RAM, I/O and functions. With memory-mapped architecture, the VLN3M can address up to 16MB space that includes memory, register files, peripheral and SPI flash storage (including instruction / data modes). SBC (Sub-Band Coding) is achieved with greatly enhanced quality & much less memory size compared against traditional ADPCM coding due to the incorporation of efficient DSP algorithms as well as the upgrade of H/W spec. Via the high performance of 32-bit MCU, the S/W-based MIDI synthesizer can reach more than 16-ch polyphonic channels. All data including SBC / MIDI files, wavetable timbres, XIP codes and general user data, can be accessed from the external SPI flash.

There are various useful features inside the VLN3M series: Three sets of 16-bit Timers; 8-ch H/W PWM-IO pins, which provide complimentary outputs (with dead zone generator) and capture feature; 8-channel, 12-bit SAR ADC with MIC pre-amplifier & AGC / PGA that supports differential MIC input; 14-bit DAC + 1.3-watt Push-Pull power amplifier to drive speaker directly; independently configurable GPIO per pin with alternate functions; IR TX that supports 38KHz / 57KHz / 125KHz / 500KHz carrier for Infrared or QFID applications; SPI0 for SPI flash control, powered by embedded optional 3.3V / 1.8V LDO, which supports single/dual/quad I/O mode with XIP (e**X**ecute **I**n **P**lace) capability; SPI1 for 2.4GHz RF module or other SPI devices; SDHC 2.0-compliant memory card; I^2C H/W interface and UART TX / RX for serial communication.

Various package forms are available for the VLN3M series: the innovative SOP-16 MCP (Multi-Chip Package), where SPI flash is stacked inside for applications that require small footprints.

2. FEATURES

- Wide Operating Voltage: 2.4V ~ 5.5V
  - SPI flash @ SPI0 powered by embedded LDO, 3.3V (default)
  - Min. operating voltage is 3.0V @ 32MHz maximum CPU clock, and 2.2V @ 12MHz minimum CPU clock.
- 32-bit CPU core
  - like ARM Cortex-M0+.
  - Max. CPU clock: 32MHz, up to 50+ DMIPS cooperated with zero wait-state high speed OTP.
  - 1-cycle fast multiplier.

- Dual Clock Operation. Built-in oscillators for HI_CLK (32MHz) and LO_CLK (32.768KHz), accuracy trimmed to +/-0.5% for HI_CLK and +/-1.5% for LO_CLK.
- Power management to support 4 operating modes: Normal / Slow / Standby / Halt mode. At Halt mode, the consumption current is less than 1uA.
- LVD (Low Voltage Detection): Total 6-level options: 3.6V, 3.4V, 3.2V, 2.6V, 2.4V, 2.2V.
- LVR (Low Voltage Reset): User-configurable, default values are 2.7V @ 32MHz for VLN3M, 2.4V @ 24MHz, 2.0V @ 16MHz, 1.8V @ 12MHz.
- Timers (Timer0 / Timer1 / Timer2): Each Timer consists of divider and 16-bit down-counter with various clock sources.
- Two PWM Generators (PWMA / PWMB)
  - Each generator consists of a clock divider, a 16-bit timer (that can be used as a general timer) and four 16-bit duty cycle registers.
  - Capture supported @ PWMA.
- ADC (Analog Digital Conversion)
  - 8-ch (with auto scan mode), 12-bit resolution SAR (Successive Approximate Register) ADC.
  - Trigger by underflow of Timer0 /1 /2, or software manually.
- Built-in MIC bias, 2-stage of pre-amplifiers and AGC/PGA for gain control.
- Built-in 14-bit DAC + 1.3-Watt Push-Pull power amplifier
  - Line-In to mix with internal analog output @ power amplifier to drive speaker.
- IR , SPI supported.
- RTC with 16KHz (or 4KHz) / 1KHz / 64Hz / 2Hz interrupts.
- WDT (Watch-Dog Timer) supported with optional 188ms / 750ms Reset.
- MCP (Multi-Chip Package)
  - SPI Flash stacked inside low-cost SOP-16 packages
  - Support 4Mb / 8Mb / 16Mb / 32Mb SPI Flash density
  - SPI0 interface bonded inside the package, leaving more GPIO pins available
  - Built-in Push-Pull PA to drive speaker directly
  - Max. GPIO pins: 8 ~ 12 @ SOP-16,
  - Master or Slave operation
- Support OTP Security Lock to prevent OTP data from being read.
- S/W-based Speech/MIDI Codec & various algorithms
  - ADPCM Codec (Adaptive Differential PCM): 4-bit / 5-bit per sample.
  - SBC Codec (Sub-Band Coding): 4.5K ~ 32Kbps with maximum 16KHz bandwidth.

- CELP Decoder (Code-Excitation Linear Prediction): 4.8Kbps @ 8KHz SR for human voice only.
- MIDI: Up to 16-channel MIDI @ 32KHz Output Sample Rate.

- Noise filter @ 4x Up-Sampling.
- Shipping Form
  - Package: SOP-16 MCP

3. PIN DESCRIPTION

Name	Type	Description
VDD	P, I	Power input
ADC_VDD	P, O	Power output for analog circuitry at VLN3M. This pin must be connected with 0.1uF cap to ground.
VSS	P, I	Ground
VMIC	AO	MIC bias
MICP	AI	MIC+
MICN	AI	MIC-
PP1/ DAC0	AO	Push-Pull PA output 1 or DAC0
PP2	AO	Push-Pull PA output 2
PA0	I/O	PA0
PA1	I/O	PA1
PA2	I/O	PA2
PA3	I/O	PA3
PA4	I/O	PA4
PA5	I/O	PA5, supported with CSC (Constant Sink Current) capability
PA6	I/O	PA6, supported with CSC (Constant Sink Current) capability
PA7	I/O	PA7, supported with CSC (Constant Sink Current) capability

Pad Type: P = Digital Power, I = Digital Input, O = Digital Output, AI = Analog Input, AO = Analog output

4. CLOCK GENERATOR

The clock generator consists of 3 clock sources:

- Built-in high clock (I_HRC): Output frequency can be 32MHz, 24MHz, 16MHz, or 12MHz by option.
- Built-in low clock (I_LRC): Output frequency is 32,768Hz.
- External crystal oscillators: 12MHz / 16MHz X'tal for HI_CLK, or 32,768Hz X'tal for LO_CLK source. Beside 12MHz / 16MHz clocks, there is a frequency doubler inside the clock generator to output 24MHz / 32MHz as well, depending on the choice of the HI_CLK.

The internal oscillators, I_HRC and I_LRC, are trimmed to achieve +/-0.5% and +/-1.5% accuracy, respectively.

5. OPERATING MODE

The VLN3M series provides four kinds of operating modes to tailor for various kinds of applications while saving power consumption. These operating modes are normal mode, slow mode, standby mode and halt mode.

Normal mode is designated for high-speed, high-performance operation, while slow mode is designated for low-speed to save power consumption. At standby mode, the VLN3M series will stop almost all operations, except

peripheral blocks with clock source from LO_CLK, to wake-up periodically. At halt mode, the VLN3M series will stop all operations, waiting for external events to wake it up.

When the VLN3M is power up, there is a delay of 32mS before user's code is executed to ensure the proper operation. Besides, the SPI Flash needs another 15mS to get power stabilized after SPI0_VDD is turned on. Therefore, there is a total of 50mS or so before any attempt to access the data stored inside the SPI Flash.

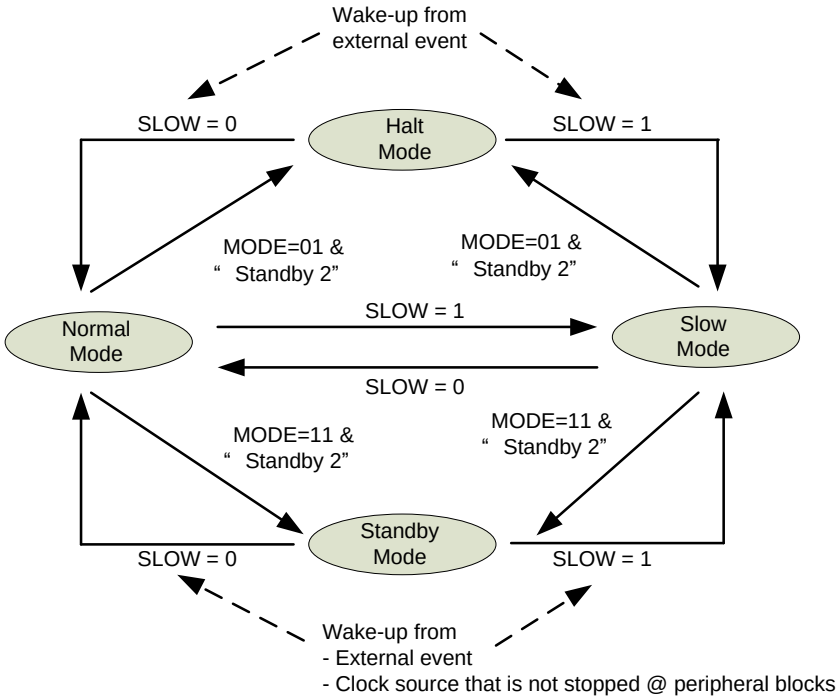


Figure 1 Four Operating Modes

6. PERIPHERALS

6.1 I/O Port

Each pin can be configured as input or output, weak / strong pull-high resistor and can generate interrupt signal to CPU. Among them, 8 pins (PA5 ~ PA7) are supported with CSC (Constant Sink Current) capability, which help keep the current thru LED constant without the current-limiting resistor.

6.2 SPI

There are two SPI masters supported. One is the SPI0 that is dedicated for connecting with an external SPI flash device to store most of the data used for various applications like speech (ADPCM, SBC, or CELP), melody (including MIDI file and wavetable timbres), user's general data storage. With single/dual/quad[1] I/O

[1] Quad I/O mode

modes supported, the SPI flash can run up to 32MHz clock. Together with the XIP capability (e**X**ecute **I**n **P**lace), users can extend the program code to the SPI flash at a descent performance for many applications. The other is the SPI1 master with single I/O mode, which can be used to interface with popular devices like 2.4GHz RF for a wireless connectivity.

For power-saving purpose, the Light-Load LDO provides merely 5mA sourcing capability, consumes only 2uA power consumption, and is used to prevent from floating @ VDD_ADC for microphone input applications, or to lower the power consumption @ slow mode. Due to limited sourcing capability @ Light-Load LDO, it can only be used for reading SPI Flash. Users may determine by S/W programming if the Light-Load LDO is required under slow / standby / halt modes.

6.3 PWM-IO

The VLN3M has 2 sets of PWM-IO generators (PWMA / PWMB). Each four PWM outputs share a PWM-Timer, every output has its own duty and output port. Besides, there are two complementary PWM pairs (PWMA0 / PWMA1) with dead zone implemented.

The VLN3M also supports capture function by using the 16-bit Timer/Counter at PWMA, where PWMA0 ~ PWMA3 is disabled when capture function enabled.

- Four PWM outputs share a 16-bit timer
- Programmable divider as the clock source of timer
- 16 bits for PWM's duty
- 8 bits for determining the length of dead zone
- Capture source is one of PA0 ~ PA7

7. TIMER

The VLN3M has three 16-bit timers: TIMER0 / TIMER1 / TIMER2, which can be used as a trigger source for DAC / PWM-IO or as a function of time delay, clock generation, etc.

- Programmable source of timer clock
- 16-bit counter for each timer

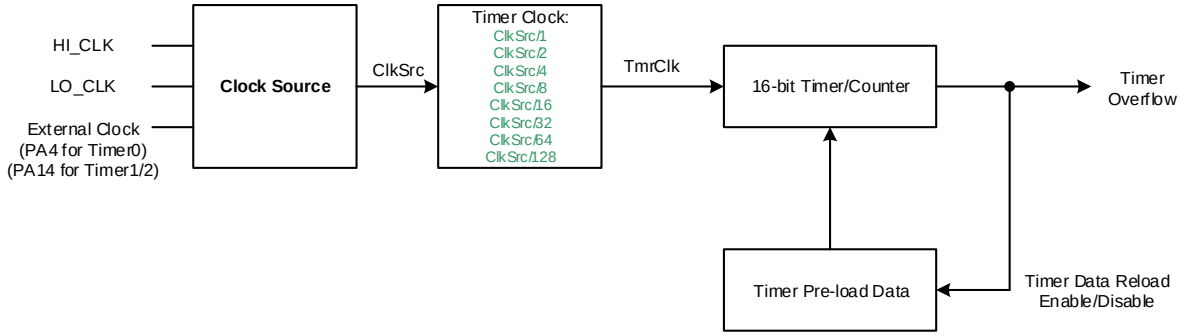


Figure 2 Timer Block Diagram

8. RTC

As the name implies, the RTC (Real-Time Clock) is generally used to keep the time, with the clock source from either an internal built-in I_LRC (trimmed to 32,768Hz with +/-1.5% accuracy), or an external crystal (32,768Hz). The RTC support periodic time tick interrupts with 4 options: 16KHz (or 4KHz), 1KHz, 64Hz, 2Hz.

9. WDT

The Watchdog Timer (WDT) is used to perform a system reset when the system is not responding. There are two period options for the WDT to generate a reset: 188ms / 750ms.

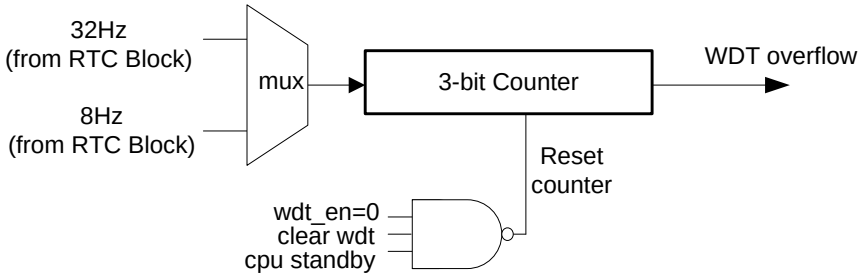


Figure 3 WDT Block Diagram

10. ADC

The VLN3M provide one 12-bit Analog-to-Digital converter with eight input channels. The A/D converter supports single and continuous scan mode. It can be started by software or TIMER trigger.

- Provide 8-level FIFO or data registers for each channel.
- Auto scan mode, which can auto get 4/3/2 channel's data by just one trigger.

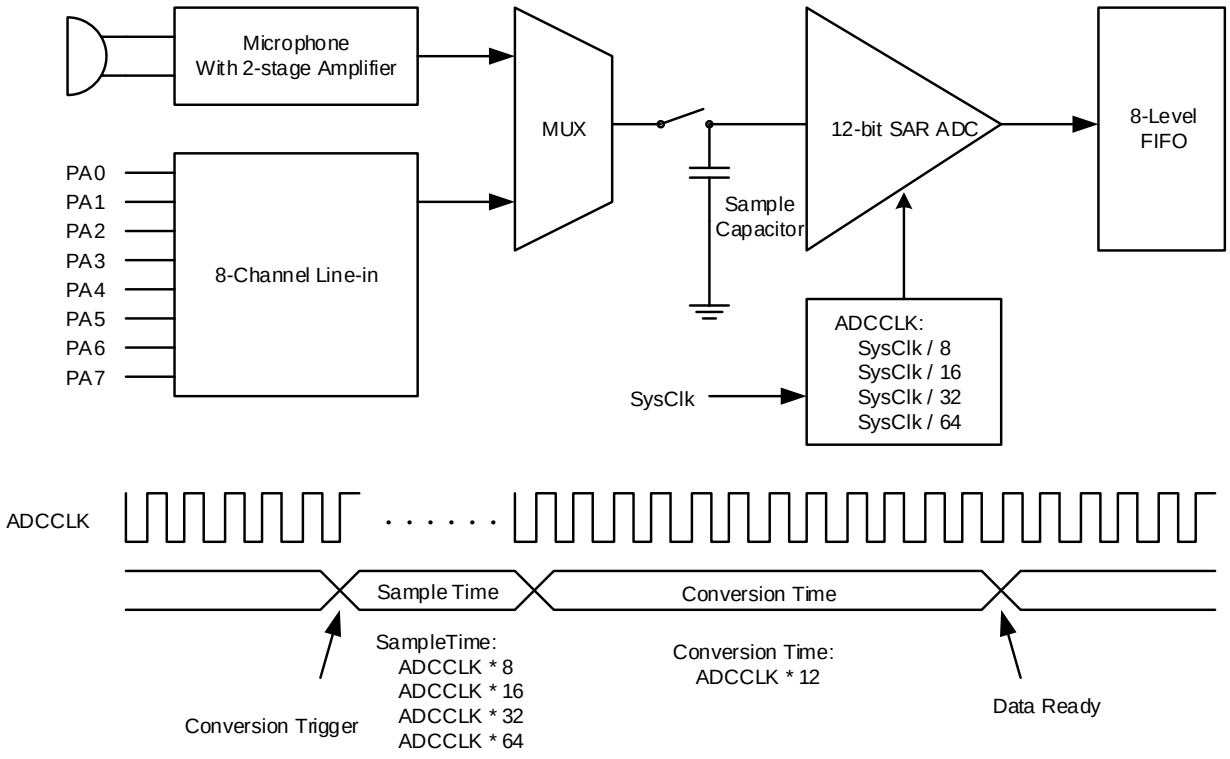


Figure 4 ADC Block Diagram

11. DAC & PP

The VLN3M provides two data buffers with 8-level FIFO each and up to two 14-bit Digital-to-Analog converters (optional) with interpolation function. It can be started by software or TIMER trigger.

- Provide 8-level FIFO per channel data buffer
- Provide hardware up-sampling (interpolation) function
- Support mixing mode for two-channel data applications

External ACIN can be mixed with internal analog output at the Push-Pull Power Amplifier stage, such that the combined analog signal could be used to drive the speaker directly.

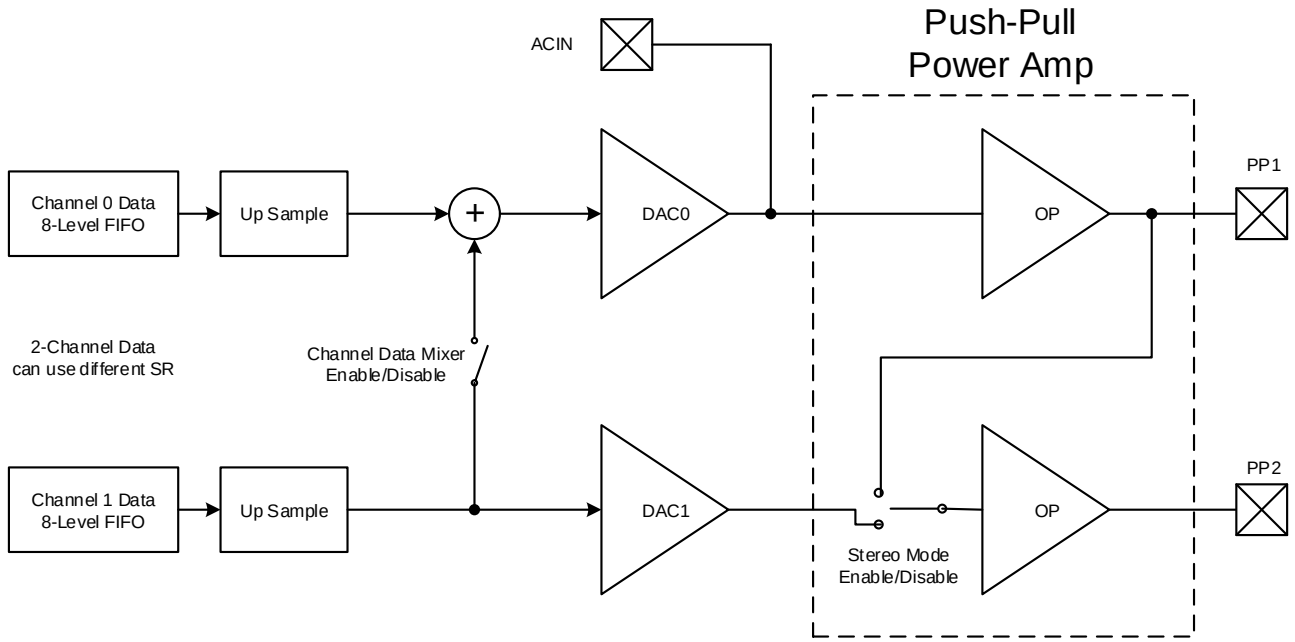


Figure 5 Block Diagram of DAC and PP PA

12. LVD

The LVD (Low Voltage Detector) is trimmed to +/-0.1V accuracy for the user to detect the battery voltage @ VDD pin. When the VDD voltage falls below the specified LVD level, the LVD_Flag will be set as HIGH.

LVD_SEL[2:0]	Voltage
111	*Reserved*
110	*Reserved*
101	3.6V
100	3.4V
011	3.2V
010	2.6V
001	2.4V
000	2.2V

Table 2 LVD voltage select

13. OPTIONS

Users may select different options depending on the application requirement. There are several options that users may select for the VLN3M series, as shown in Table 3 User Options.

Item	Name	Options
1	High Oscillation Source	1. I_HRC 2. E_HXT

2	Low Oscillation Source	1. I_LRC 2. E_LXT
3	HI_CLK Frequency	1. 32MHz (Core LDO @ 3.3V) 2. 24MHz (Core LDO @ 2.7V / 2.8V) 3. 16MHz (Core LDO @ 2.3V / 2.5V) 4. 12MHz (Core LDO @ 2.3V / 2.5V)
4	VDD Voltage	1. 4.5V 2. 3.0V
5	SPI0_VDD Voltage	1. 3.3V 2. 1.8V
6	LVR Voltage	1.2.6V / 2.5V / 2.4V / 2.3V / 2.2V (HI_CLK @ 24MHz) 2. 2.2V / 2.1V / 2.0V / 1.9V / 1.8V (HI_CLK @ 16MHz) 3. 2.0V / 1.9V / 1.8V / 1.7V / 1.6V (HI_CLK @ 12MHz)

Table 3 User Options

14. ELECTRICAL CHARACTERISTICS

14.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
V_{DD} - V_{SS}	Supply voltage	-0.5 ~ +7.5	V
V_{IN}	Input voltage	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
T_{OP}	Operating Temperature	0 ~ +70	°C
T_{ST}	Storage Temperature	-25 ~ +85	°C

14.2 DC Characteristics *(T_A=25ºC, unless otherwise specified)*

Symbol	Parameter		V_{DD}	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage		-	3.0	4.5	5.5	V	CPU_CLK=32MHz
				2.7	4.5	5.5		CPU_CLK=24MHz
				2.2	3.0	5.5		CPU_CLK=16MHz
				2.2	3.0	5.5		CPU_CLK=12MHz
				2.2	3.0	5.5		CPU_CLK=32.768KHz
I_{HALT}	Halt Current		3		0.1		uA	CPU stop, all functions off, Disable SPI0_VDD[*1]
			4.5		0.1			
			3		1.1		uA	CPU stop, all functions off, Enable SPI0_VDD[*1]
			4.5		1.3			
I_{SB}	Standby Current		3		3.5		uA	CPU stop, all functions off, RTC on, Enable SPI0_VDD[*1]
			4.5		4.5			
I_{OP}	Operating Current	Slow Mode	3		58.3		uA	CPU_CLK=32.768KHz, Enable SPI0_VDD[*1]
			4.5		75			
		Normal Mode	3		6.1		mA	CPU_CLK = 12MHz, Core_LDO = 2.3V, Enable SPI0_VDD[*2]
			3		7.5		mA	CPU_CLK = 16MHz, Core_LDO = 2.3V, Enable SPI0_VDD[*2]
			4.5		12.0		mA	CPU_CLK = 24MHz, Core_LDO = 2.7V, Enable SPI0_VDD[*2]
			4.5		19.1		mA	CPU_CLK = 32MHz, Core_LDO = 3.3V, Enable SPI0_VDD[*2]

Symbol	Parameter		V_{DD}	Min.	Typ.	Max.	Unit	Condition
I_{IL}	Input current (Internal pull-high)	Weak (1MΩ)	3		-2.7		uA	V_{IL} = 0V
			4.5		-7.2			
		Strong (100KΩ)	3		-30			
			4.5		-78			
		SDC pad (20KΩ)	3		-144			
			4.5		-215			
I_{OH}	Normal drive current (PA, PB[7:6], PB[15:12])		3		-8.7		mA	V_{OH} = 2.0V
			4.5		-13.7			V_{OH} = 3.5V
	Normal drive current (SPI0, SPI1, SDC)		3		-12.9			V_{OH} = 2.0V
			4.5		-20.2			V_{OH} = 3.5V
	Large drive current (SPI0, SPI1, SDC)		3		-24.8			V_{OH} = 2.0V
			4.5		-38.0			V_{OH} = 3.5V
I_{OL}	Normal sink current		3		12.4		mA	V_{OL} = 1.0V (CSC, constant sink current, not for VLN3M1P21A and VLN3M1M)
			4.5		19.2			
	Large sink current		3		24.3			
			4.5		37.1			
	Normal constant sink current (PA[15:8])		3		13			
			4.5		13			
	Large constant sink current (PA[15:8])		3		20			
			4.5		20			
I_{PP}	Push-Pull Output Current		3		180*3 200*4		mA	Load = 8Ω
			4.5		280*3 300*4			
ΔF/F	Frequency deviation by voltage drop (I_HRC=32MHz/24MHz)		4.5		-0.5		%	Fosc(4.5v) - Fosc(3.3v) / Fosc(4.5v)
	Frequency deviation by voltage drop (I_HRC=16MHz/12MHz)		3		-0.5			Fosc(3.0v) - Fosc(2.4v) / Fosc(3.0v)
			4.5		-0.5			Fosc(4.5v) - Fosc(3.0v) / Fosc(4.5v)
			4.5		280*3 300*4			
ΔF/F	Frequency deviation by lot		3	-0.5		0.5	%	Fosc(3.0v) - Ftyp(3.0v) / Ftyp(3.0v)

*[*1] Light-Load LDO @ SPI0_VDD is rated at 5mA for lowering power consumption @ Halt, Standby, and Slow modes.*

*[*2] Heavy-Load LDO @ SPI0_VDD is rated at 40mA for read / erase / write operation to the SPI Flash @ Normal mode.*

14.3 ADC Characteristics *(V_{DD}=3.3V, T_A=25ºC, unless otherwise specified)*

Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{INL}	ADC LINE_IN Input Voltage Range from PA[7:0]	V_{SS} - 0.3		V_{DD} + 0.3	V
V_{INM}	ADC Microphone Input Voltage Range	V_{SS} - 0.3		V_{DD} + 0.3	V
B_{RES}	Resolution of ADC			12	Bit
ENOB	Effective Number of Bits		10		Bit
INL	Integral Non-Linearity of ADC		+/-4		LSB
DNL	Differential Non-Linearity of ADC		+1.5 / -0.9		LSB
F_{CONV}	AD Conversion Rate			SYS_CLK/184	Hz

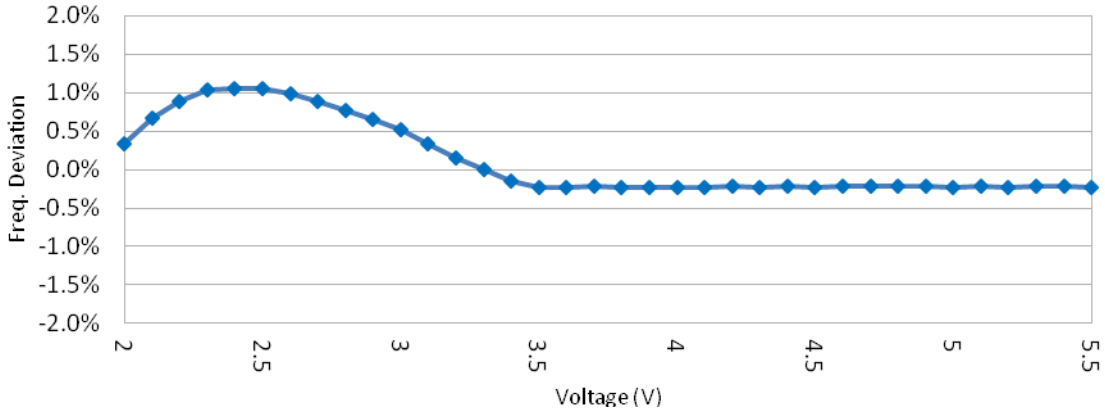
14.4 DAC Characteristics *(V_{DD}=5V, T_A=25ºC, unless otherwise specified)*

Symbol	Characteristics	Min.	Typ.	Max.	Unit	Condition
B_{RES}	Resolution of DAC			14	Bit	-
DR	Dynamic Range (Vin = -60 dBFS)		-73		dBr A	No Load
SNR	Noise at No Signal (Vin = -90 dBFS)		-97		dBr A	
P_O	THD+N 1%		0.7		W	4Ω Load
	THD+N 10%		1.3*[*1]		W	

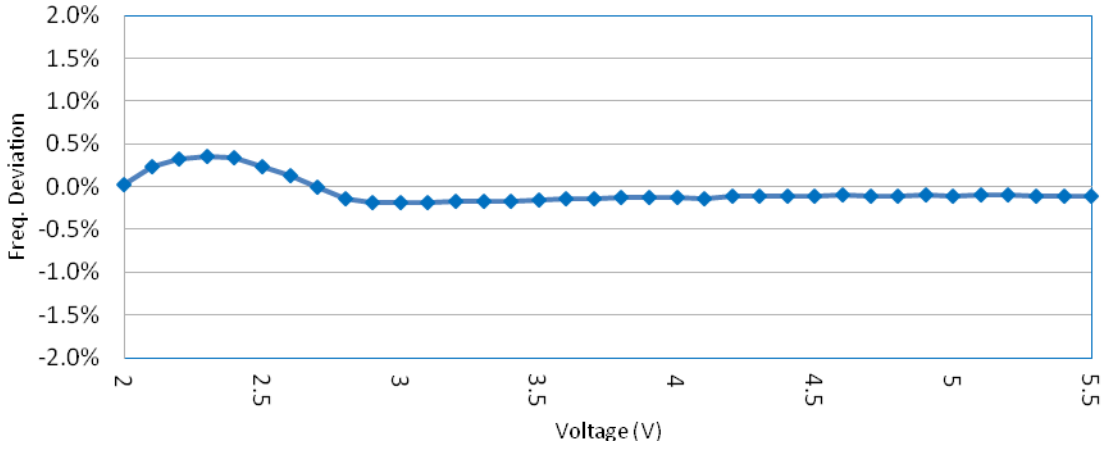
*[*1] 1.3-Watt for VLN3MxxS16X*

14.5 Voltage vs. Frequency

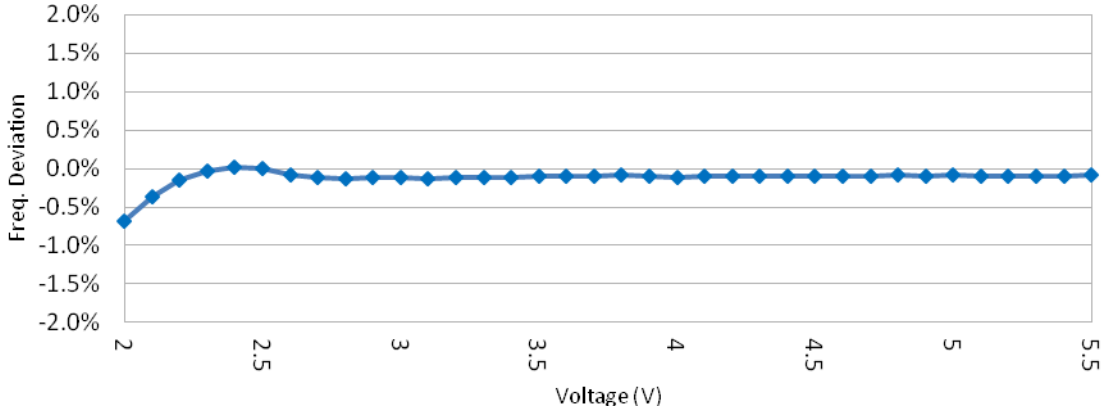
14.5.1 I_HRC @ 32 MHz



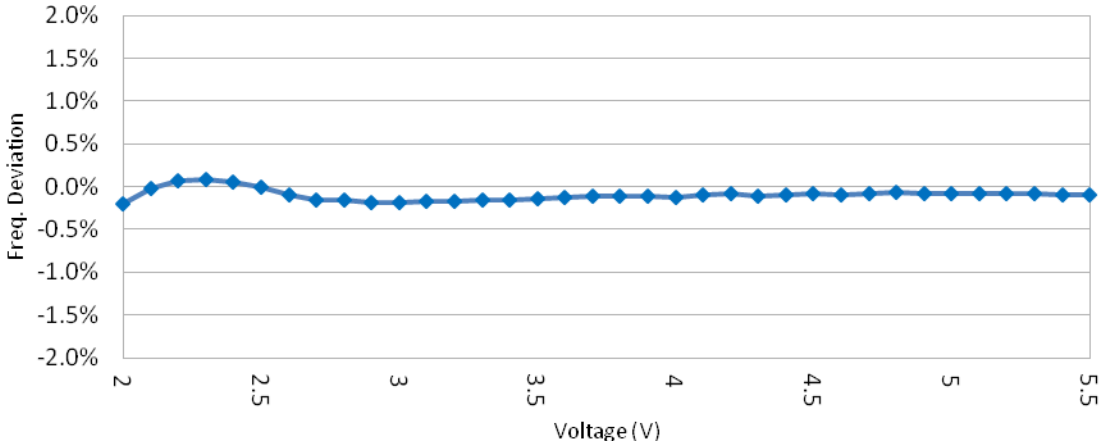
14.5.2 I_HRC @ 24 MHz



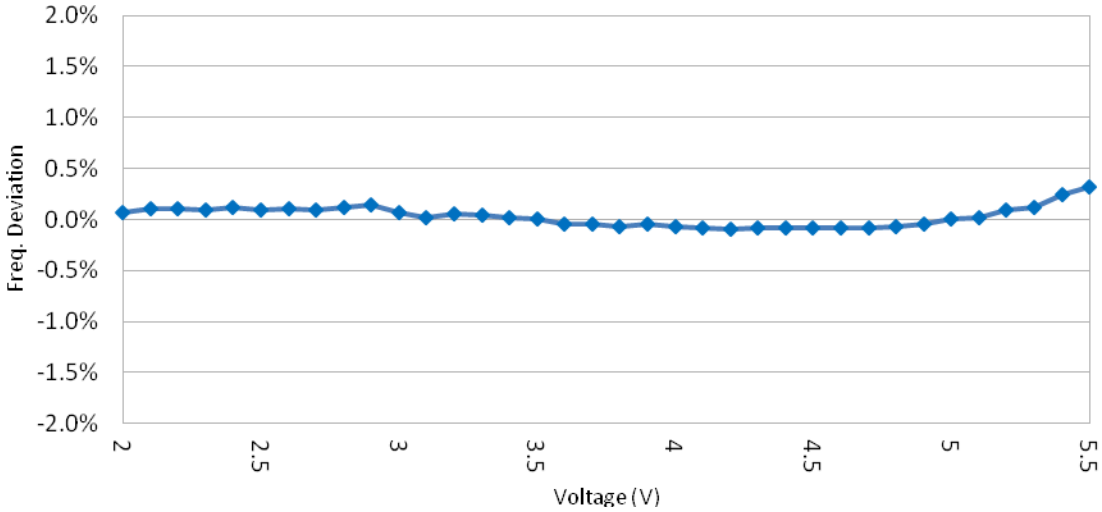
14.5.3 I_HRC @ 16 MHz



14.5.4 I_HRC @ 12 MHz

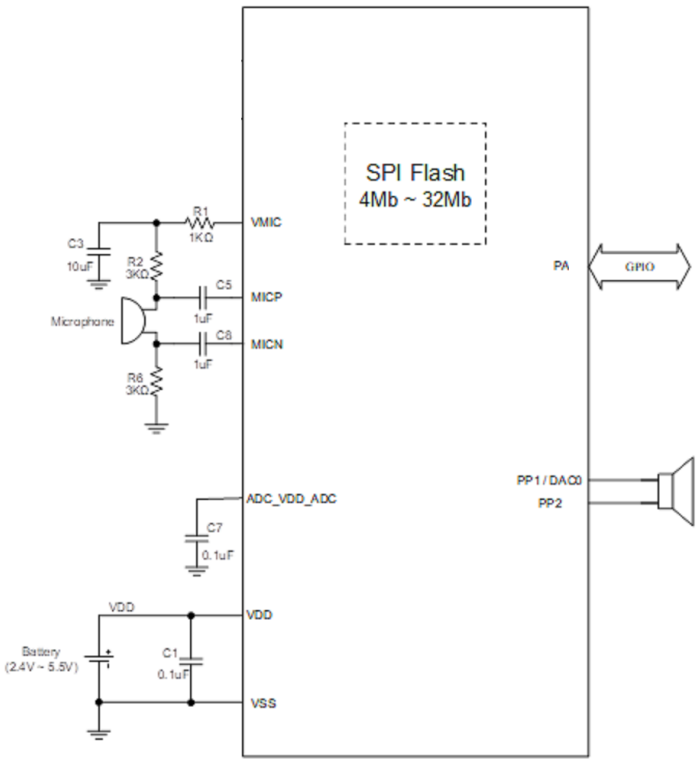


14.5.5 I_LRC @ 32 KHz



15. APPLICATION

15.1 VLN3MxxS16X

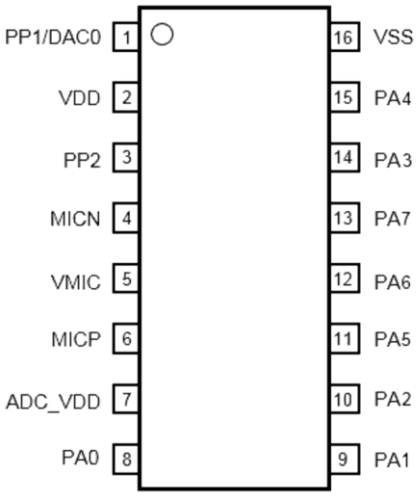


Note 1: For IHRC crystal @ 16MHz / 12MHz, do NOT add the compensation capacitors at Xin / Xout pins.

16. PACKAGE PIN ASSIGNMENT

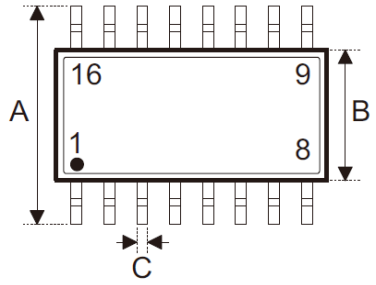
16-pin SOP (150mil)

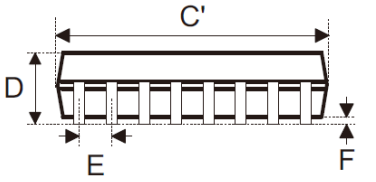
VLN3MxxS16X



17. PACKAGE DIMENSION

17.1 SOP-16 (150mil, 1.27mm pin pitch)





	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A		0.236 BSC			6.00 BSC	
B		0.154 BSC			3.90 BSC	
C	0.012	-	0.020	0.31	-	0.51
C'		0.390 BSC			9.90 BSC	
D	0.065	-	0.069	1.64	-	1.75
E		0.050 BSC			1.27 BSC	
F	0.004	-	0.010	0.10	-	0.25
G	0.016	-	0.050	0.40	-	1.27
H	0.004	-	0.010	0.10	-	0.25
α	-	-	8°	-	-	8°

Note: For 16-pin SOP IC, 50 units per tube.

18. ORDERING INFORMATION

P/N	*Shipping Type*	*Remark*
VLN3M08S16X	SOP-16 (MCP)	Width 150 mil, pitch 1.27mm
VLN3M32S16X	SOP-16 (MCP)	Width 150 mil, pitch 1.27mm