DATA SHEET

VL4P Series *(OTP)*

Single-Chip 4-bit MCU with 1-Ch Speech & 8 I/O

Version 1.21

Jan. 5, 2011

Revision History

Version	Date	Description	Modified Page
1.0	2010/9/08	Formally release.	-
1.1	2010/10/20	Modify PWM2 to PMW2/Mode.	11
1.2	2011/1/05	1. Add Chinese description for Chapter 1 & 2. 2. External OSC pad “PX#/OSC” is connected to V_{REG} pad.	3, 4 11, 15

1. GENERAL DESCRIPTION

The VL4P series IC is a powerful 4-bit micro-controller based sound processor. They are embedded EPROM architecture, and the OTP (One Time Programmable) ICs that are designed to support VLN4A and VLN4B MaskROM products. There is only 1-channel speech with high quality direct-drive PWM output. By using the high fidelity ADPCM speech synthesis algorithm and a built-in noise filter, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz is supported. The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 44 instructions, and most of them are executed in single cycle. Furthermore, a HALT mode (sleep mode) is designed to minimize power dissipation. Through +/-1% accurate internal oscillation, external Rosc is unnecessary.

2. FEATURES

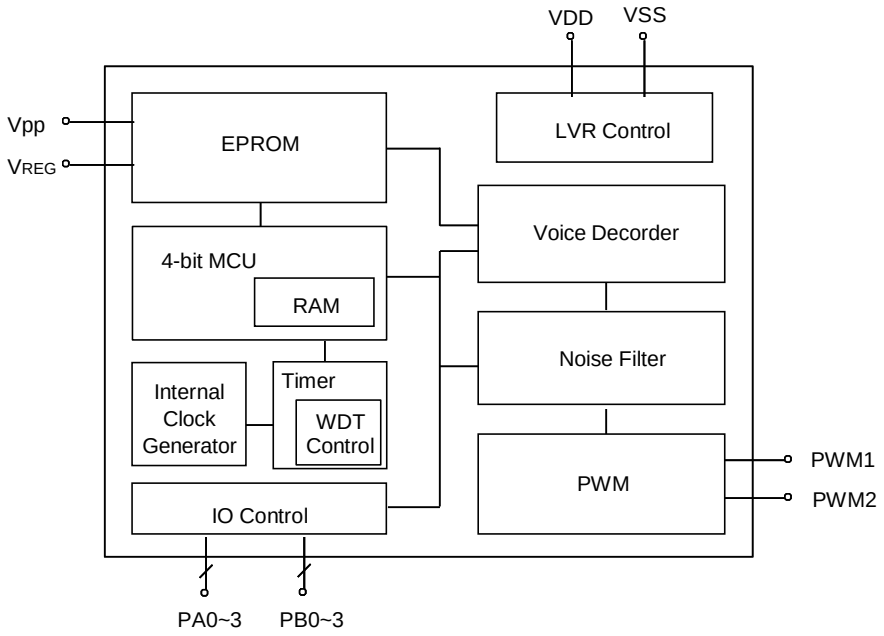
- Wide operating voltage range: 2.0V to 5.5V. *(Same as MaskROM products)*
- 4-bit RISC type micro-controller with 44 instructions.
- 256Kx10-bit ROM maximum, program and voice data share the same ROM space. The voice duration, ROM size and I/O counts are shown below.

Product (OTP)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
VLN005-4P	5.0	16k x 10	8
VLN018-4P	18.3	48k x 10	8
VLN045-4P	45.0	112k x 10	8
VLN065-4P	65.0	160k x 10	8
VLN105-4P	105.0	256k x 10	8

- 96x4-bit RAM, divided into 2 pages.
- 1MHz instruction frequency.
- HALT mode to save power, less than 1uA standby current.
- Precisely embedded oscillator with build-in resistor Rosc (+/- 1%).
- Low voltage reset *(LVR=1.8V)*, watch-dog reset and I/O port reset are all supported to protect the system.
- Maximum 8 flexible I/Os with optional function: floating, pull-high, strong / weak pull-high, Reset input, IR carrier output. I/O's direction is controlled by registers. For the output port, users can select the normal Drive current output or large Sink current output to directly drive high brightness LED.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- New high fidelity ADPCM speech synthesis algorithm.
- Built-in noise filter for less background noise at lower volume especially.
- One 9-bit hardware PWM output.

- Support large PWM current output.
- Mute mode speech algorithm to save ROM size.
- Quick-IO control supported.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP (In Circuit Programming) writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*
- Various shipping type for different application requirement.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

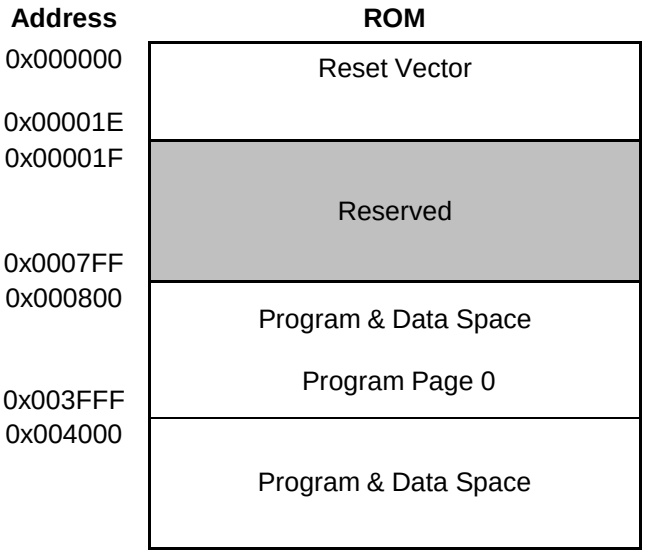
Pad Name	ATTR.	Description
Vpp	Power	Positive high power for programming.
V_{REG}	Power	Regulator input. Connect a 0.1uF cap to GND or keep floating.
VDD1~2	Power	Positive power.
GND1~2	Power	Negative power.
PA0/SDA	I/O	Bit 0 for Port A, or serial data input at programming mode.
PA1/SCL	I/O	Bit 1 for Port A, or serial clock input at programming mode.
PA2/IR	I/O	Bit 2 for Port A, or IR transmitter pin.
PA3/Reset	I/O	Bit 3 for Port A, or external reset pin.
PB0~1	I/O	Bit 0~1 for Port B.
PB2/IR	I/O	Bit 2 for Port B, or IR transmitter pin.
PB3/Reset	I/O	Bit 3 for Port B, or external reset pin.
PWM1	O	PWM1 output.
PWM2/Mode	O	PWM2 output, or select programming mode.

5. MEMORY ORGANIZATION

There are maximum 256K words EPROM, 96 nibbles of RAM and 14 nibbles of dedicated system control register. Besides, there are several registers without address allocation, and they can only be accessed by the special instructions. One of the registers is RAM page register (PG), and the other one is 8-bit sample rate timer (TM).

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 14-bit length address of ROM, the program page size is 16K words.



5.2 RAM

Each page of RAM contains 48 nibbles, and VL4P serial provides 96 nibbles of 2 pages. The page number (PG) register of RAM defined by the MPG instruction, and its initial value is 0. The address for RAM is 0x10~0x3F.

6. CLOCK GERERATOR

The clock generator is a Ring oscillator, and users can only select the internal resistor (INT-R). The INT-R oscillator accuracy is up to ±1%.

7. IO PORTS

There are 8 I/O pins at most, designated as PAx through PBx, and x=0~3. All the I/O ports can be configured as input or output by registers. For the input port, we provide an internal pull-high register option for convenience. For the output port, users can select the large sink current output or normal drive current output.

A reset port can possess a pull-high resister or not, and an IR port can be large sink current or normal drive current output.

The pull-high resister of all the I/O ports has two kinds of option: weak and strong. The weak one is about 750kΩ @3V for normal application and the strong one is about 33kΩ @3V usually for key matrix function. When users configure the weak or strong pull-high resister, the pull-high resisters of all I/O ports are set as the option value.

8. AUDIO SYNTHESIZER

There is 1-ch voice, and all modes are auto-played back by hardware. One audio output stages: 9-bit PWM is supported. The VLN4 series supports 9-bit PCM and encoded ADPCM speech data. Of course, the PCM speech has higher quality and occupies more ROM space than the ADPCM one. Use the encode software provided by the VoiceLand to generate the PCM or ADPCM speech data. The voice start address is loading to VPR when executing the PLAY command.

There is an option of normal PWM current or large PWM current for different customer demand. The large PWM current consumes more current and makes sound louder. *(VLN4A don't support the large PWM output.)*

A Noise-Filter is built-in. When users enable this option, hardware will suppress the noise to reduce the background noise automatically. Users can also disable this option up to the sound source.

A voice channel includes a PFLG, a VPR, a voice decoder, a QIO control code generator and an 8-bit sample rate timer (TM) whose timer clock source (TCS) is fixed to 1MHz. It supports PCM and encoded ADPCM speech data.

The VLN4 series supports another special mute mode for speech. When a speech like the vocal or talk has a lot of suspension or silence, using the mute mode saves much ROM space. Turn on the mute mode option of the encode software to save your cost.

9. ELECTRICAL CHARACTERISTICS

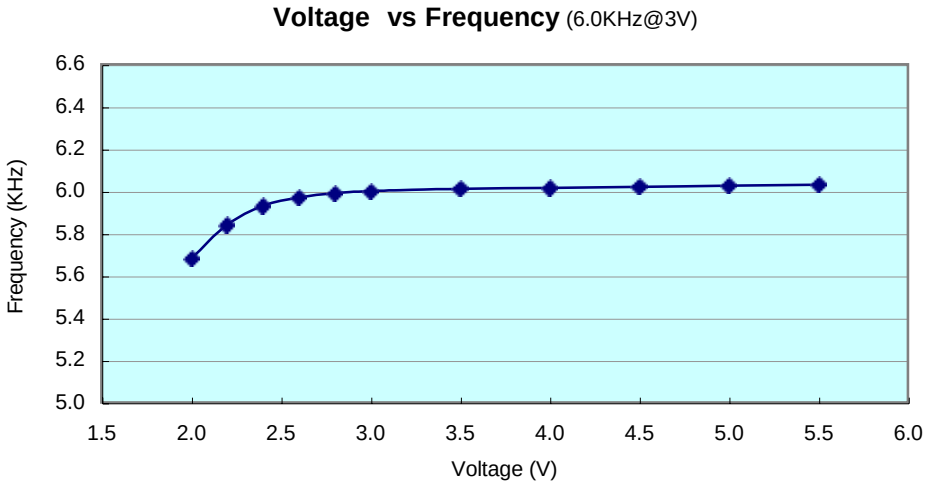
9.1 Absolute Maximum Rating

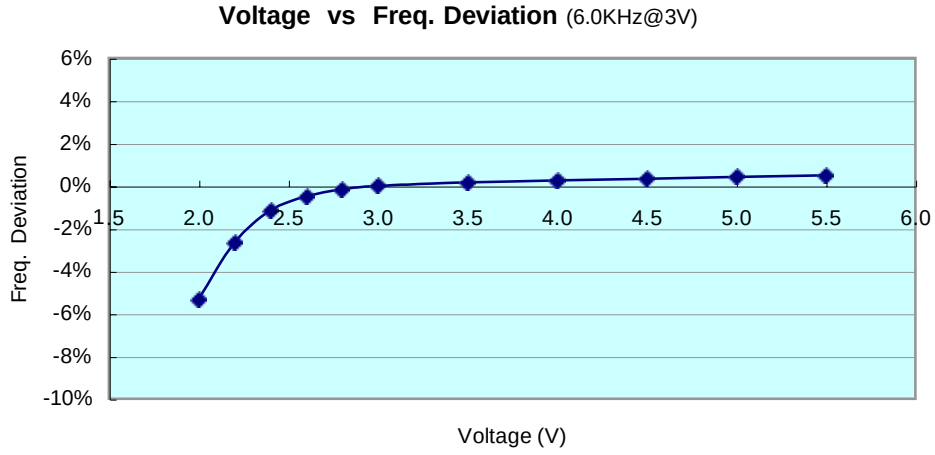
Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

9.2 DC Characteristics

Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	1 MHz
Isb	Supply current	Halt mode	3			1	uA	Sleep, no load
			4.5			1		
Iop		Operating mode	3		1.8		mA	1MHz, no loading
			4.5		2.7			
Iil	Input current (Internal pull-high)	Weak (750k ohms)	3		-3.7		uA	Vil=0v
			4.5		-10			
		Strong (33k ohms)	3		-67			
			4.5		-170			
Ioh	Output high current		3		-7		mA	Voh=2.0V
			4.5		-11			Voh=3.5V
Iol	Output low current (Large current)		3		17		mA	Vol=1.0V
			4.5		26			Vol=1.0V
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
I_{PWM}	PWM output current (Large)		3		70		mA	Load=8 ohms
			4.5		117			
△F/F	Frequency deviation by voltage drop (1MHz)		3		2		%	Fosc(3.0v)-Fosc(2.4v) / Fosc(3v)
			4.5		1			Fosc(4.5v)-Fosc(3.0v) / Fosc(4.5v)
△F/F	Frequency lot deviation (1MHz)		3	-1		1	%	Fmax(3.0v)-Fmin(3.0v) / Fmax(3.0v)
Fosc	Oscillation Frequency		-	0.90	1	1.05	MHz	VDD=2.0~5.5V

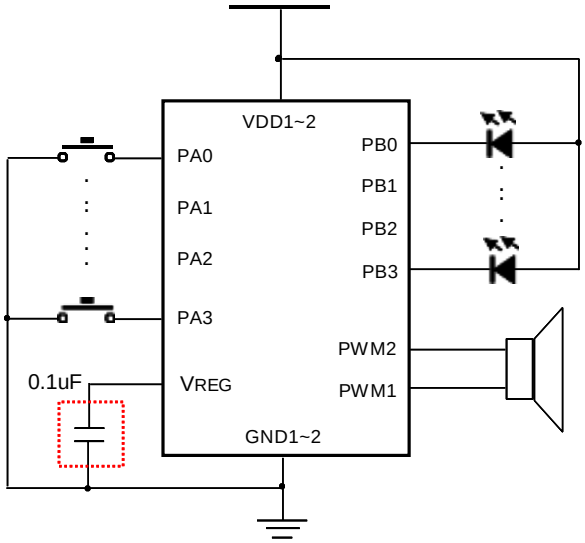
9.3 Voltage vs. Frequency



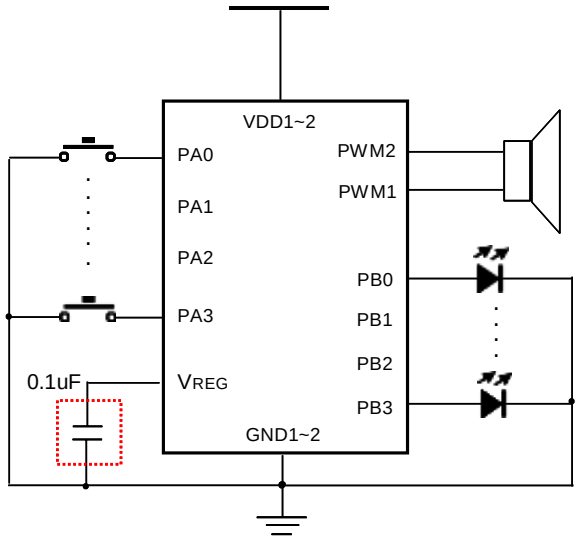


10. APPLICATION

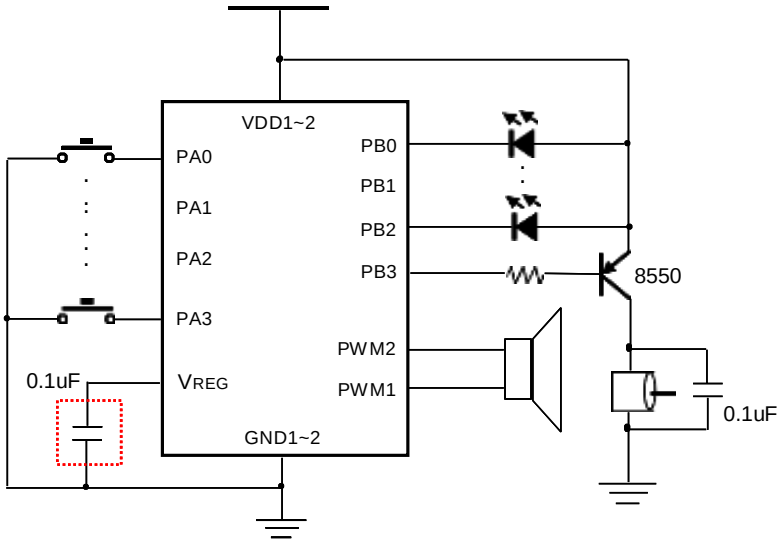
(1) INT-R, PWM, Sink output with 4 LEDs



(2) INT-R, PWM, Drive output with 4 LEDs

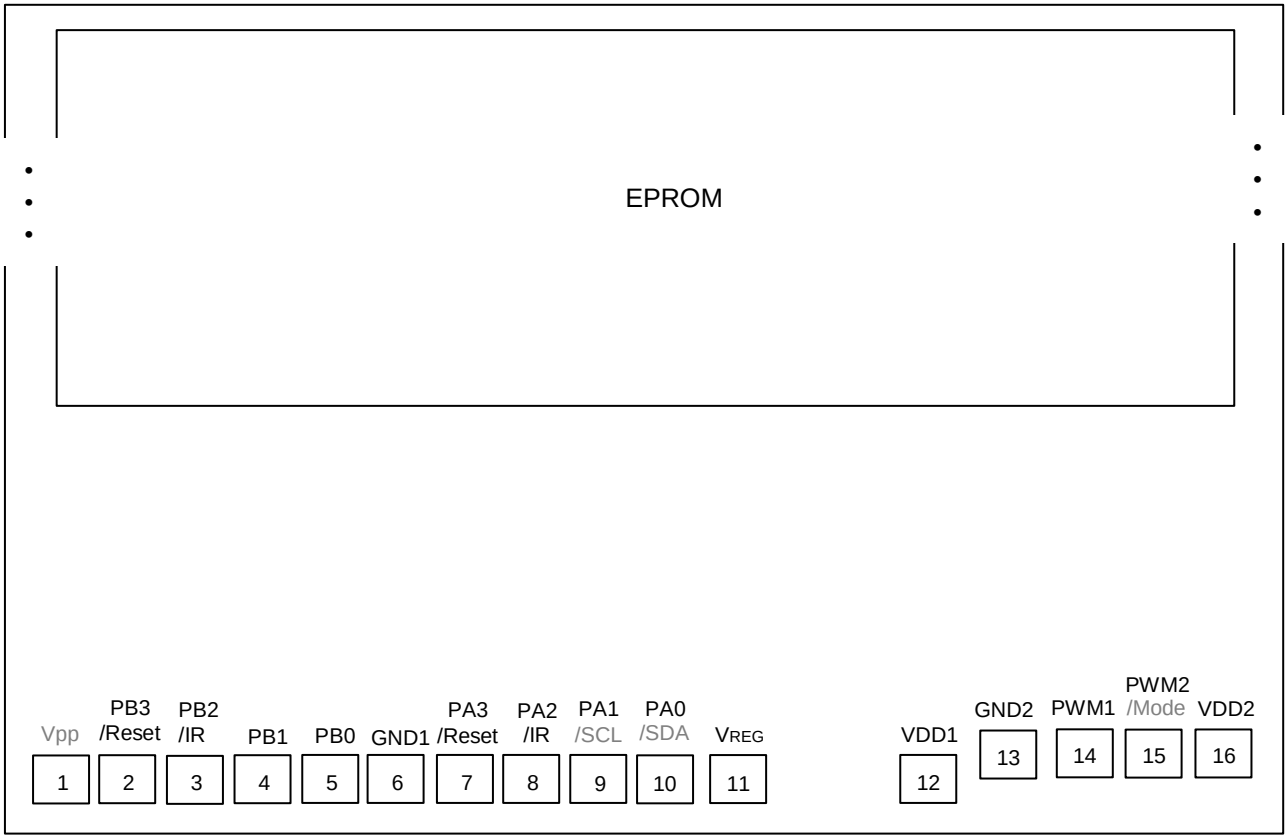


(3) INT-R, PWM, Sink output with 3 LEDs and 1 Motor



Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

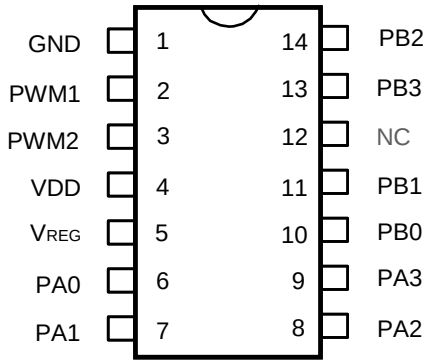
11. DIE PAD DIAGRAM



12. COB

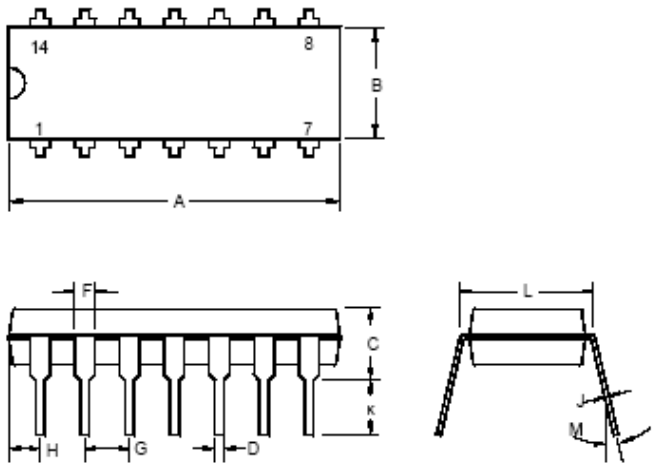
13. PACKAGE PIN ASSIGNMENT

14-pin DIP, SOP



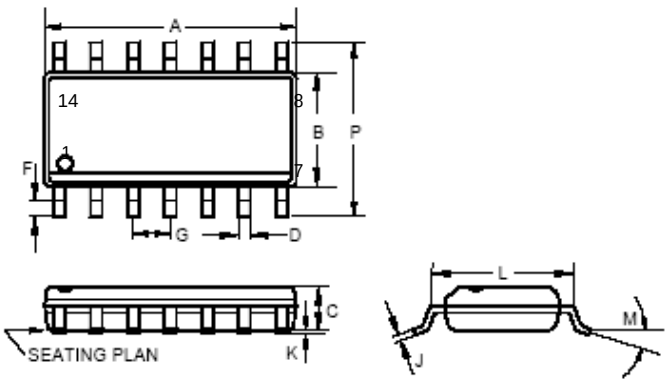
14. PACKAGE DIMENSION

14-Pin Plastic DIP (300 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.730	-	0.810	18.54	-	20.57
B	0.240	-	0.260	6.09	-	6.60
C	-	-	0.200	-	-	5.08
D	0.015	-	0.020	0.38	-	0.51
F	0.03	-	0.060	0.76	-	1.52
G	0.100 BSC			2.54 BSC		
H	0.050	-	0.090	1.27	-	2.28
J	0.008	-	0.015	0.20	-	0.38
K	0.125	-	-	3.18	-	-
L	0.300 BSC			7.62 BSC		
M	-	-	15°	-	-	15°

14-Pin Plastic SOP (150 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.337	-	0.344	8.55	-	8.75
B	0.144	-	0.163	3.66	-	4.14
C	0.068	-	0.074	1.73	-	1.88
D	0.017	-	0.020	0.35	-	0.51
F	0.016	-	0.044	0.40	-	1.12
G	0.050 BSC			1.27 BSC		
J	-	0.004		-	0.10	-
K	0.005	-	0.010	0.13	-	0.25
L	0.189	-	0.205	4.80	-	5.21
M	-	-	8°	-	-	8°
P	0.228	-	0.244	5.80	-	6.20

15. ORDERING INFORMATION

P/N	Shipping Type	Remarks
VLN005-4P	Die	Empty ROM data
VLN005-4P-xxxx *1	Die	Programmed ROM data
VLN005-4PW-xxxx *1	Wafer	Programmed ROM data
VLN005-4PB	COB	20 mm x 19 mm (20mm x 24 mm w/ V-Cut)
VLN005-4PP14	DIP-14	Width 300 mil
VLN005-4PS14	SOP-14	Width 150 mil
VLN018-4P	Die	Empty ROM data
VLN018-4P-xxxx *1	Die	Programmed ROM data
VLN018-4PW-xxxx *1	Wafer	Programmed ROM data
VLN018-4PB	COB	20 mm x 19 mm (20mm x 24 mm w/ V-Cut)
VLN018-4PP14	DIP-14	Width 300 mil
VLN018-4PS14	SOP-14	Width 150 mil
VLN045-4P	Die	Empty ROM data
VLN045-4P-xxxx *1	Die	Programmed ROM data
VLN045-4PW-xxxx *1	Wafer	Programmed ROM data
VLN045-4PB	COB	20 mm x 19 mm (20mm x 24 mm w/ V-Cut)
VLN045-4PP14	DIP-14	Width 300 mil
VLN045-4PS14	SOP-14	Width 150 mil
VLN065-4P	Die	Empty ROM data
VLN065-4P-xxxx *1	Die	Programmed ROM data
VLN065-4PW-xxxx *1	Wafer	Programmed ROM data
VLN065-4PB	COB	20 mm x 19 mm (20mm x 24 mm w/ V-Cut)
VLN065-4PP14	DIP-14	Width 300 mil
VLN065-4PS14	SOP-14	Width 150 mil
VLN105-4P	Die	Empty ROM data
VLN105-4P-xxxx *1	Die	Programmed ROM data
VLN105-4PW-xxxx *1	Wafer	Programmed ROM data
VLN105-4PB	COB	20 mm x 19 mm (20mm x 24 mm w/ V-Cut)
VLN105-4PP14	DIP-14	Width 300 mil
VLN105-4PS14	SOP-14	Width 150 mil

**1 "xxxx": Code number*